AMENDMENTS TO THE CLAIMS

1.-5. (Canceled).

6. (Currently Amended) An image processing device for carrying out a dodging treatment, comprising:

a luminance image signal generator for generating a luminance image signal from input color image signals;

a filter for filtering said luminance image signal to generate an unsharp image signal;

a dynamic range compressor for subjecting said unsharp image signal to a dynamic range compression treatment to generate a compressed unsharp image signal for the dodging treatment;

at least one memory for delaying said input color image signals for a time period corresponding to a delay time ~~during which~~ of said compressed unsharp image signal for the dodging treatment, thereby generating delayed input color image signals, said delay time occurring as a result of processing of ~~is generated from~~ said input color image signals;

an adder for subtracting said compressed unsharp image signal for the dodging treatment from each of said delayed input color image signals to generate processed image signals for the dodging treatment.

7. (Previously Presented) The device according to claim 6, wherein said filter is an IIR type filter.

8. (Currently Amended) The device according to claim 6, wherein said at least one memory comprises a plurality of FIFO type field memories disposed in parallel, and while said input color image signals are sequentially written to one FIFO type field memory ~~and~~, said delayed input color image signals are sequentially read-out from one other FIFO type field memory, ~~sequentially~~ and, alternatively, while said input color image signals are sequentially written to said one other FIFO type field memory, said delayed input color image signals are sequentially read-out from said one FIFO type field memory.

9. (Currently Amended) The device according to claim 6, further comprising, a main controller for generating reading and writing signals which control writing to and reading from said at least one memory to control ~~the~~ operation ~~time~~ timing of said at least one memory in accordance with the delay time of said input color image signals at said filter.

10. (Currently Amended) The device according to claim 9, wherein said main controller includes a first counter which counts a number of pixels in horizontal and vertical directions of a reproduced image; a first flip-flop which generates said ~~signals controlling~~ writing signal during a time period from when said first counter starts counting until the end of counting; a second counter which starts counting a number of horizontal and vertical delays of said input color image signals at said filter, beginning when said first counter starts

counting; a third counter which starts counting the number of horizontal and vertical delays of said input color image signals at said filter, after said first counter has finished counting; and a second flip-flop which generates said ~~signals controlling~~ reading signal after said second counter has finished counting, and until a time period when said third counter finishes counting.

11. (Previously Presented) The device according to claim 7, wherein said IIR type filter is at least one of a low-pass filter and an all-pass filter.

12. (Previously Presented) The device according to claim 6, wherein said luminance image signal generator is a matrix calculator.

13. (Previously Presented) The device according to claim 6, wherein said dynamic range compressor subjects to said dynamic range compression treatment using a dynamic range compression table.